What is claimed is:

1. A simultaneous bi-directional (SBD) buffer which includes a self-test circuit having a function of generating an input signal, the SBD buffer comprising:

an output driver which receives an output data signal and outputs the received output data signal to an input/output node;

an input receiver which receives a signal generated after combining an input data signal inputted to the input/output node with the output data signal, compares the signal with a reference voltage, and outputs a comparison result;

a first multiplexer which outputs the reference voltage in response to a reference voltage selection signal; and

an input signal generating circuit which generates an input signal used for testing in a test mode and outputs the input signal used for testing as the input data signal.

2. The SBD buffer of claim 1, wherein the reference voltage selection signal is either the output data signal or a first control signal.

3. The SBD buffer of claim 2, wherein the SBD buffer further comprises a second multiplexer which outputs either the output data signal or the first control signal as the reference voltage selection signal in response to a test mode activation signal activated in the test mode.

4. The SBD buffer of claim 2, wherein the input signal generating circuit comprises:

a multiplexer which outputs a signal having a predetermined voltage level in response to a second control signal;

an output driver which receives an output signal of the multiplexer and outputs the input signal used for testing to the input/output node; and

a switching means which is connected between the output driver and the input/output node, is switched in response to an enable signal activated in the test mode, and outputs the input signal used for testing to the input/output node.

5. The SBD buffer of claim 4, wherein the input signal used for testing has either an internal voltage level or a ground voltage level.

6. The SBD buffer of claim 2, wherein the input signal generating circuit comprises:

a delay circuit which delays the output data signal for a predetermined amount of time and outputs the input signal used for testing to the input/output node; and

a switching means which is connected between the delay circuit and the input/output node, is switched in response to the enable signal activated in the test mode, and outputs the input signal used for testing to the input/output node.

7. The SBD buffer of claim 6, wherein the input signal used for testing has either an internal voltage level or a ground voltage level.

8. The SBD buffer of claim 1, wherein a voltage level of an input signal inputted to the input receiver changes according to voltage levels of the output data signal and the input signal used for testing in the test mode.

9. The SBD buffer of claim 8, wherein the input signal inputted to the input receiver has one of the internal voltage level, half the internal voltage level, and the ground voltage level in the test mode.

10. The SBD buffer of claim 1, wherein the reference voltage is either 3/4 times the internal voltage or 1/4 times the internal voltage.

11. A self-test method of a simultaneous bi-directional (SBD) buffer which includes a self-test circuit having a function of generating an input signal, the method comprising:

(a) outputting an output data signal to an input/output node;

(b) selecting a voltage level of a reference voltage in response to a reference voltage selection signal;

(c) generating an input signal used for testing in a test mode and outputting the generated input signal used for testing to the input/output node; and

(d) comparing a signal generated by combining the output data signal with the input signal used for testing with the reference voltage and outputting the comparison result.

12. The method of claim 11, wherein the input signal used for testing has either the internal voltage level or the ground voltage level.

13. The method of claim 11, wherein the signal generated by combining the output data signal with the input signal used for testing has one of the internal voltage level, half the internal voltage level, and the ground voltage level.

14. The method of claim 11, wherein the reference voltage is either 3/4 times the internal voltage or 1/4 times the internal voltage.